424 Rec'd PCT/PTO 21 JUN 2000

FORM PTO-1390 (Modified) (REV 11-98) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: 000394

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR): 09/582067

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE98/03794	18 December 1998	22 December 1997

TITLE OF INVENTION

Semiconductor Substrate with Embedded Insulating Layer for Integrated Circuits

APPLICANT(S) FOR DO/EO/US

Erzgraeber et al.

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ A copy of the International Search Report (PCT/ISA/210).
8. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
9. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
10. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
11. ☒ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☒ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 13 to 20 below concern document(s) or information included:

13. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☒ Certificate of Mailing by Express Mail
20. ☒ Other items or information:

Assignee's Certificate of Small Entity Status;
a Post Card Receipt

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/582067	PCT/DE98/03794	000394

21. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

		CALCULATIONS PTO USE ONLY
☐	Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO and International Search Report not prepared by the EPO or JPO	**$970.00**
☒	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but Internation Search Report prepared by the EPO or JPO	**$840.00**
☐	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO	**$690.00**
☐	International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4)	**$670.00**
☐	International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4)	**$96.00**

ENTER APPROPRIATE BASIC FEE AMOUNT =				ă	**$840.00**
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).				ă	**$0.00**
CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	8 - 20 =	0	x $18.00	ă	**$0.00**
Independent claims	ă 2 - 3 =	0	x $78.00	ă	**$0.00**
Multiple Dependent Claims **(check if applicable)**.			☐	ă	**$0.00**
TOTAL OF ABOVE CALCULATIONS =				ă	**$840.00**
Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28) **(check if applicable)**.			☒	ă	**$420.00**
SUBTOTAL =				ă	**$420.00**
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). +				ă	**$0.00**
TOTAL NATIONAL FEE =				ă	**$420.00**
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).**			☒	ă	**$40.00**
TOTAL FEES ENCLOSED =				ă	**$460.00**
				Amount to be: refunded	$
				charged	$

☒ A check in the amount of **$460.00** to cover the above fees is enclosed.

☐ Please charge my Deposit Account No. Òă in the amount of ă to cover the above fees.
A duplicate copy of this sheet is enclosed.

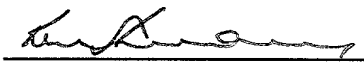
☐ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. ă A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Law Offices of Karl Hormann
86 Sparks Street
Cambridge, MA 02138-2216

Tel.: (617)-491-8867



SIGNATURE

Karl Hormann

NAME

26,470

REGISTRATION NUMBER

20 June 2000

DATE

CERTIFICATE OF MAILING BY "EXPRESS MAIL" (37 CFR 1.10) Applicant(s): **Erzgraeber et al.**			Docket No. **000394**
Serial No. 09/582067	Filing Date **21 June 2000**	Examiner	Group Art Unit **PCT**

Invention: **Semiconductor Substrate with Embedded Insulating Layer for Integrated Circuit**

I hereby certify that the following correspondence:

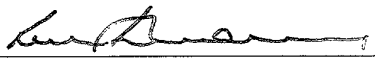
Application to Commence the U.S. National Phase of PCT/DE98/03794

(Identify type of correspondence)

is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 in an envelope addressed to: The Assistant Commissioner for Patents, Washington, D.C. 20231 on

21 June 2000
(Date)

Karl Hormann
(Typed or Printed Name of Person Mailing Correspondence)



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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

International Application No.: PCT/DE98/03794
International Filing Date: 18 December 1998
Inventor: Erzgräber et al.
For: Semiconductor Substrate with Embedded...

86 Sparks Street
Cambridge MA 02138-2216
20 June 2000

Hon.
Assistant Commissioner for Patents
Washington DC 20371

Box PCT

Preliminary Amendment Prior to Claims Fee Calculation

Sir:

With a view to putting the instant application as amended pursuant to Rule 66 of the Patent Cooperation Treaty into a condition believed formally to comply with U.S. prosecution standards and to avoid excess claims fees otherwise due, applicants courteous request entry of the following amendment.

In the Specification:

Page 1, line 7: insert --BACKGROUND OF THE INVENTION.

1. Field of the Invention.--;

line 18: insert --2. The State of the Art.--;

page 3, line 5: cancel "is";

line 18: insert --OBJECTS OF THE INVENTION.--;

line 26: insert --SUMMARY OF THE INVENTION.--;

page 5, line 17: insert --DESCRIPTION OF THE DRAWINGS.--;

line 28: insert --DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS.--;

page 8: line 2: cancel "Patent Claims" and substitute --What is claimed is-- therefor; and

page 11, line 2: cancel "Abstract" and substitute --ABSTRACT OF THE DISCLOSURE.-- therefore.

In the Claims:

Claim 1, line 1: change "Integrated" to --An integrated--;

claim 2, line 1: change "Integrated" to --The integrated-- and "characterized by the fact" to --wherein--;

line 2: after "µm" insert --is--;

claim 3, line 1: change "Integrated" to --The integrated-- and "characterized by the fact that" to --wherein--;

line 3: change "and" to --an--;

claim 4, line 1: change "Method" to --A method--;

line 2: after "with" insert --a--;

line 3: change "characterized by" to --comprising--;

claim 5, line 1: change "Method" to --The method-- and "characterized by" to --further comprising--;

claim 6, line 1: change "Method" to --The method-- and "or 5, characterized by" to --, further comprising the step of--;

claim 7, line 1: change "Method" to --The method-- and "one or more of claims" to --claim-- and cancel "to 6, characterized by the";

line 2: change "fact that" to --wherein--; and

claim 8, line 1: change "Method" to --The method-- and "one or more of

claims" to --claim-- and cancel "to 6, characterized by the";

line 2: change "fact that" to --wherein--.

Respectfully submitted,

Karl Hormann
Registration No.: 26,470

Area Code (617)-491-8867

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) AND 1.27 (c)) - SMALL BUSINESS CONCERN	Docket No. 000394

Serial No.	Filing Date	Patent No.	Issue Date

Applicant/ Patentee: **Erzgraeber et al.**

Invention: **Semiconductor Substrate with Embedded Insulating Layer for Integrated Circuits**

I hereby declare that I am:

- ☐ the owner of the small business concern identified below:
- ☒ an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF CONCERN: **Institut fuer Halbleiterphysik Frankfurt (Oder) GmbH.**

ADDRESS OF CONCERN: **Im Technologiepark 25, D-15236 Frankfurt/Oder, Germany**

I hereby declare that the above-identified small business concern qualifies as a small business concern as defined in 13 CFR 121.3-18, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees under Section 41(a) and (b) of Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the above identified invention described in:

- ☒ the specification filed herewith with title as listed above.
- ☐ the application identified above.
- ☐ the patent identified above.

If the rights held by the above-identified small business concern are not exclusive, each individual, concern or organization having rights to the invention is listed on the next page and no rights to the invention are held by any person, other than the inventor, who could not qualify as an independent inventor under 37 CFR 1.9(c) or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern or organization to which I have assigned, granted, conveyed, or licensed or am under an obligation under contract or law to assign, grant, convey, or license any rights in the invention is listed below:

☒ no such person, concern or organization exists.
☐ each such person, concern or organization is listed below.

FULL NAME _____
ADDRESS _____

☐ Individual ☐ Small Business Concern ☐ Nonprofit Organization

FULL NAME _____
ADDRESS _____

☐ Individual ☐ Small Business Concern ☐ Nonprofit Organization

FULL NAME _____
ADDRESS _____

☐ Individual ☐ Small Business Concern ☐ Nonprofit Organization

FULL NAME _____
ADDRESS _____

☐ Individual ☐ Small Business Concern ☐ Nonprofit Organization

Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING: _____

TITLE OF PERSON SIGNING

OTHER THAN OWNER: _____

ADDRESS OF PERSON SIGNING: Im Technologiepark 25
D-15236 Frankfurt/Oder, Germany

SIGNATURE: _____ DATE: May 29, 2000

Prof. A. Ourmazd F. Weinl

Directors

Integrated Circuit with Reduced Parasitic Capacitive Influence and Method of Its Fabrication

The invention relates to an integrated circuit with reduced parasitic capacitive influence and to a method of its fabrication.

The reduction of parasitic capacitive influence is of ever increasing significance particularly in modern CMOS technologies. If integrated circuits are being realized by bipolar technologies, substrate-inherent capacitive and ohmic losses of inductances or other passive circuit elements may be kept low by the use of high-ohmic or semi-insulating substrates. It mus, however, be assumed that CMOS technologies are preferred because of lower costs, low power consumption and small dimensions.

The integration of passive elements, such as, for instance, inductances constitutes a pressing necessity, particularly for realizing monolithic RF transceiver switching circuits on silicon substrates. In the GHz range impedance matching for which such passive elements are necessary. If CMOS technologies satisfy the requirements for fabricating RF transceivers for cellular systems or LAN, this means, however, that because of the usually used low-ohmic Si substrates (typically 1 - 10 Ωcm) the desired high qualities of the inductances cannot be attained a priori. Optimizing these passive components, above all, is a matter of maximizing the quality factor by minimizing resistance losses and capacitive parasitics. Substrate-inherent losses may be reduced by removing the spiral path of the inductance as far as possible from the silicon substrate, for instance, by using, in a multi-layer conductor system, the uppermost layer(s) for the spiral so that, overall, a

sufficiently thick insulation between spiral and substrate is yielded because of several intermediate plane insulating layers. However, since CMOS technologies measuring ≤ .5 µm utilize relatively thin insulating layers, the losses in low-ohmic silicon substrates cannot be kept sufficiently low without additional means. For reducing substrate-inherent losses such variants as the use of high-ohmic silicon wafers, the use of SOI substrates (on high-ohmic silicon wafer bases), the use of SOS substrate, removal of silicon below the spiral (air bridge), the use of dielectric materials of low relative dielectric constant, e.g., silicon dioxide as polymers, have been proposed. It has also been proposed to realize the metal spiral in a metal layer of a thickness of several µm over a very thick insulating layer, both layers being additionally formed above the CMOS structure required for the circuits. Such variants suffer from the drawback that established CMOS technologies must be modified or that the semiconductor substrates are dearer. Moreover, these variants cannot generally be used for all other passive elements of an integrated circuit, such as, in particular, resistors, capacitors, conductors and bonding pads which also are subject being influenced by parasitic capacitances.

U.S. Patent 5,548,150 discloses a field effect transistor on a SOI substrate in which for the purpose of increasing the velocity a buried insulating layer is arranged below the active layers for forming the active elements. Further applications of specific SOI substrates fabricated by wafer bonding relate to the fabrication of integrated inductances. Since the silicon is removed in the area of the spirals, undesirable differences in height will result. In alternatives, porous (and, therefore, high-ohmic) Si is used in other embodiments for reducing parasitics.

U.S. Patent 4,910,1165 relates to a SOI process utilizing oxidized porous silicon for forming dielectric insulating epitaxial silicon islands in which active elements are subsequently realized. Here, too, an improvement in the

velocity of field effect and bipolar transistor is brought about by reducing the direct capacitive coupling between the epitaxial Si island and the substrate by a thicker insulating layer.

A thick oxidized porous silicon layer on a p-silicon substrate is for planar inductances and other passive components is described by C. M. Nam et al. in "High Performance Planar Inductor on Thick Oxidized Porous Silicon Substrate", IEEE Microwave and guided wave letters, vol. 7, No. 8, pp. 236 seq. The thick insulating layer is formed as a large surface so that this substrate cannot be the starting point for a CMOS or CMOS compatible process. U.S. Patent 5,736,749 discloses an integrated circuit including an inductance. The inductance is formed above an area of porous silicon at least 200 µm thick. That corresponds to a local high-ohmic substrate area. The use of a high-ohmic substrate is one of the essential possibilities to reduce parasitic capacitances. It is not available, however, at a large wafer diameter and requires additional technological processes for latchup suppression.

It is an object of the invention to propose an integrated circuit of reduced parasitic capacitive influences, and a method of its fabrication, in which the parasitic capacitive influences are reduced in respect of individual elements of the integrated circuit. Furthermore, the technological sequence for realizing the contact and conductor system of modern CMOS technologies is not to be adversely affected, and additional planarizing steps are not to become necessary.

The object is accomplished by a partial insulating layer of a thickness of at least 5 µm which is locally restricted to the area of specific passive elements of the integrated circuit and which is buried in the semiconductor substrate.

The losses arising from parasitic influences and which are dependent upon the specific electrical resistance of the silicon substrate used, are significantly reduced, so that the quality of an integrated inductance may be increased as a function of the selected thickness of the buried insulating layer by about 40 % and more, relative to planar inductances based on conventional CMOS.

The essential advantage of the insulating variant here proposed resides in the realization of the thick buried oxide realized free of stresses restricted to the area of but one subsequently formed passive element of the integrated circuit. In this manner, large differences in the structural heights and, therefore, complex planarizing measures are avoided in the subsequent technological process. Therefore, the process of fabricating strongly scaled CMOS or BiCMOS structures is not adversely affected by the necessity of inserting additional thick insulating layers between the spiral and the substrate to realize integrated inductances of high quality. The fabrication of integrated circuits in accordance with the invention is accomplished by the following steps

- masking of the surface of the silicon wafer,
- forming moats and ribs by anisotropic etching,
- an optional sacrificial oxidation, i.e. a partial anoxidation of the ribs followed by oxide removal for optimizing the ratio between the widths of the ribs and the moats,
- total oxidation of the ribs to silicon oxide and at least filling of the moats adjacent to the surfaces by precipitating silicon dioxide,
- CMOS process or CMOS-compatible silicon process for the fabrication of the individual elements of the integrated circuit by utilization of the partial steps inherent in the given process for fabricating the elements of the integrated circuit, the passive elements of reduced parasitic influences being formed above the area of the buried thick oxide.

The advantage offered by the invention is that substrate-inherent losses of passive elements such as, for example, inductances, capacitances or resistances are significantly reduced. It is of particular advantage that all processes applied for fabricating the buried oxide area are CMOS compatible and thus do not include any unconventional method steps. Hence, established CMOS or CMOS compatible silicon technologies need not be modified, and a cost-efficient semiconductor substrate may be utilized. Especially in cases where CMOS technologies of structural dimensions of < .5 µm and very low ohmic substrates (< .1·cm) are used for latchup suppression, the use of the buried local insulation for integrated inductances is advantageous. In these substrates the Q factor and the inherent resonance frequency may be increased by at least 100 %. The solution in accordance with the invention may in general be applied to all other passive elements of an integrated circuit such as, in particular, resistances, capacitances, conductors and bonding pads which are also subject to parasitic capacitive influences.

The characteristics of the invention are not only apparent from the claims but also from the description and the drawings, protection being sought for elements constituting patentable embodiments by themselves or as subcombinations. Embodiments of the invention will hereinafter be explained in greater detail.

In the figures:

Fig. 1 is a schematic top elevation of the structure of an inductance;
Fig. 2 is a schematic cross-section of an inductance.

Fig. 1 is a schematic top elevation depicting the structure of an inductance as part of an integrated circuit in accordance with the invention. Fig. 2 schematically depicts a cross-section of the inductance. The integrated

inductance consists of an upper metal plane 1 for realizing a spiral, an insulating layer 2, a lower metal plane 3 for forming a contact of the internal connection 10, an insulating layer 4, a field oxide layer 5, a channel stop layer 6, a buries thick local insulating layer 7 as well as a semiconductor substrate 8. The field oxide layer 5 as well as the channel stop layer 6 are disposed only outside of the area of the integrated inductance. The buried thick local insulating layer 7 is arranged within the area of the inductance below the metal layers 1 and 3.

For fabricating the inductance, moats of a depth of about 10 µm, but at least a depth of 5 µm, are formed by anisotropic etching in a silicon wafer by means of an etching mask in the area of an integrated inductance to be formed in the subsequent process, i.e. alternating moats and ribs are being formed. The width of the ribs and moats is selected such that during subsequent transformation of the ribs into silicon oxide by a thermal oxidizing process the moats are closed by for a residual width of about 100 nm to 300 nm. Because of the increase in volume, ribs of a width of .8 µm and moats of a width of 1.2 µm will yield residual moats of a width of about 150 nm to 200 nm following total oxidation. Optionally, the ratio of the width of ribs and moats may be precisely realized by a preceding sacrificial oxidation or partial anoxidation of the ribs followed by removal of the oxide for reducing the width of the Si ribs and enlarging the width of the moats. The entire array of parallel moats and ribs is surrounded by a moat which is wider by about 25 %. This moats prevents prestresses, particularly at the ends of the long Si ribs during their transformation. The residual moats remaining after total oxidation are closed completely, at least near their surface, by a subsequent precipitation of silicon dioxide, for instance by a CVD process. This sequence results in a thick buried insulating layer 7 the thickness of which is defined by the depth of the etched moats. The cavities remaining in the middle area of this oxide region offer the additional advantage of an effectively reduced dielectric constant. Removal of the CVD oxide layer from the surface and of the

etching mask for etching the moats is followed by the appropriate CMOS or CMOS compatible silicon process. Alternatively, the etching mask may be partially or completely removed prior to oxidation of the ribs. The integrated inductance is realized above the buried thick insulating layer 7 by using the contact and conductor system present in the CMOS process.

An integrated circuit of reduced parasitic capacitive influences and a method of its fabrication have been set forth by the present invention on the basis of a concrete example. It is to be noted, however, that the present invention is not limited to the details of the embodiments in the description as changes and mutations are being claimed within the scope of the claims. An insulating layer locally restricted to the area of the elements of the integrated circuit and buried in the semiconductor substrate is not only suitable for fabricating an integrated inductance, but also other elements of the integrated circuit, in particular further passive components such as resistors and capacitors as well as conductors and bonding pads.

Patent Claims:

1. Integrated circuit of reduced parasitic capacitive influences comprising an insulating layer (7) buried in the semiconductor substrate (8), characterized by the insulating layer (7) being at least 5 µm thick and is locally restricted to specific areas of the integrated circuit, i.e. to specific passive elements.

2. Integrated circuit according to claim 1, characterized by the fact that the partial insulating layer (7) of a thickness of at least 5 µm locally restricted to the area of one or more integrated inductances, one or more integrated resistors, one or more integrated capacitors, one or more integrated bonding pads and/or one or more conductors and buried in the semiconductor substrate (8).

3. Integrated circuit according to claim 2, characterized by the fact that the integrated inductance consists of at least one upper metal plane (1) for realizing a spiral, and insulating layer (2), a lower metal plane (3) for forming a contact of the inner connector (10), an insulating layer (4), a field oxide layer (5), a channel stop layer (6), a buried local insulating layer (7) of a thickness of at least 5 µm as well as a semiconductor substrate (8).

4. Method of fabricating an integrated circuit by means of CMOS or CMOS compatible silicon technologies with local buried insulation, characterized by the method steps

- masking of the surface of the silicon wafer,
- forming moats of a depth of at least 5 µm and ribs in a width ratio of about 3.2 as well as a moat wider by about 25 % drawn around the entire array of moats and ribs, by anisotropic etching,
- an optional sacrificial oxidation, i.e. a partial anoxidation of the ribs

followed by oxide removal for precisely optimizing the ratio between the widths of the ribs and the moats for the purpose of reducing prestresses and possible formation of displacement in the successive process step,

- total oxidation of the ribs to silicon oxide and at least filling of the remaining moats adjacent to the surfaces by precipitating silicon dioxide, whereby cavities remain in the middle area of the oxide area which offer the additional advantage of an effectively increased dielectric constant,
- CMOS process or CMOS-compatible silicon process for the fabrication of the individual elements of the integrated circuit by utilization of the partial steps inherent in the given process for fabricating the elements of the integrated circuit, passive elements of the integrated circuit being formed for the purpose of reduced parasitic influences directly above the area of the buried insulation layer (7) of at least 5 µm thickness.

5. Method according to claim 4, characterized by the process steps of

- masking of the surface of the silicon wafer,
- forming moats at least 5 Mm deep and ribs by anisotropic etching,
- an optional sacrificial oxidation, i.e. a partial anoxidation of the ribs followed by oxide removal for optimizing the ratio between the widths of the ribs and the moats,
- total oxidation of the ribs to silicon oxide and at least filling of the moats adjacent to the surfaces by precipitating silicon dioxide,
- CMOS process or CMOS-compatible silicon process for the fabrication of an inductance above the area of the buried thick oxide using the contact and conductor system present in the given process.

6. Method according to claim 4 or 5, characterized by etching moats of a depth of at least 5 µm, the width of the ribs and moats being selected such that during a subsequent complete transformation of the ribs into silicon

dioxide by oxidation the moats are closed but for a residual width of about 100 nm to 300 nm.

7. Method according to one or more of claims 4 to 6, characterized by the fact that moats of at least 5 µm depth are etched such that ribs of a width of about .8 µm and moats of a width of about 1.2 µm are formed and that this array of moats and ribs is surrounded by a wider moat of a width of about 1.5 µm.

8. Method according to one or more of claims 4 to 6, characterized by the fact that the moats of a depth of at least 5 µm are etched such that ribs of a width of about .8 µm and moats of a width of about 1.2. µm are subsequently formed by an additional sacrificial oxidation step.

Abstract

The invention relates to an integrated circuit of reduced parasitic capacitive influences and to a method of its fabrication. It is an object of the invention to propose an integrated circuit of reduced parasitic capacitive influences and a method of its fabrication in which the parasitic capacitive influences for individual especially passive elements of the integrated circuit is reduced. In addition, the technological sequence for realizing the contact and conductor system of modern CMOS or CMOS compatible silicon technologies is not to be adversely affected during the fabrication of circuits with integrated passive elements and, in particular, no additional planarizing steps are to become necessary. The object is accomplished by an at least partial insulating layer of a thickness of at least 5 µm which is locally restricted to the area of the elements of the integrated circuit and which is buried in the semiconductor substrate. The losses caused by parasitic influences and dependent upon the specific electrical resistance of the silicon substrate used, are significantly reduced so that depending upon the selected thickness of the buried insulating layer, the quality of an integrated inductance may be improved by about 40 % or more relative to planar inductances based upon conventional CMOS.

09/582067

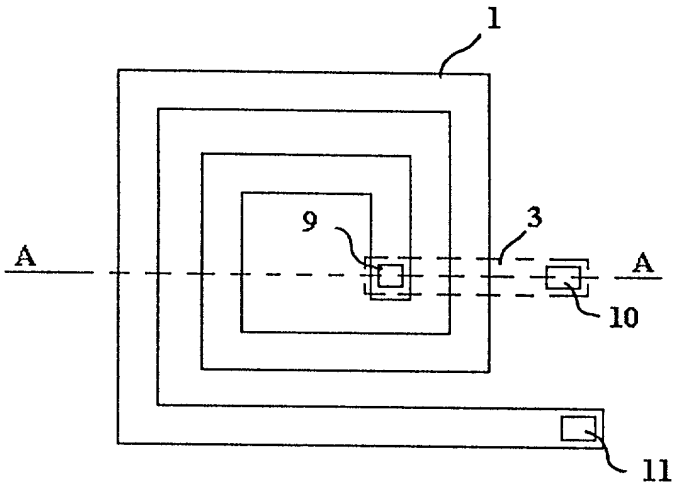

Fig. 1

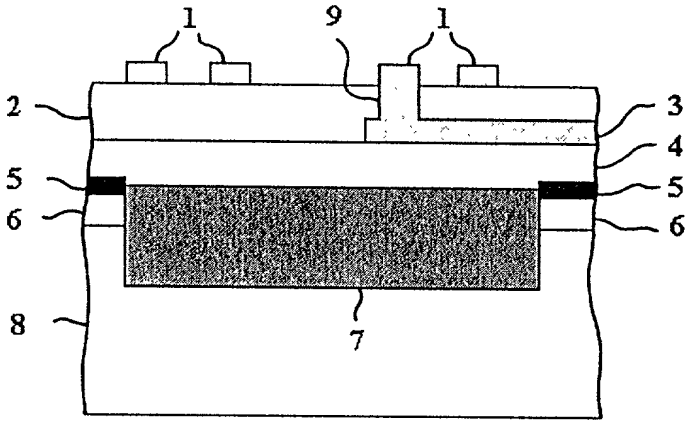

Fig. 2

Docket No.
000394

Declaration and Power of Attorney For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Semiconductor Substrate with Embedded Insulating Layer for Integrated Circuits

the specification of which

(check one)

☒ is attached hereto.

☐ was filed on _____ as United States Application No. or PCT International Application Number _____

and was amended on _____

(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Not Claimed
197 58 349.0	Germany	22 December 1997	☐
(Number)	(Country)	(Day/Month/Year Filed)	
198 47 440.7	Germany	8 October 1998	☐
(Number)	(Country)	(Day/Month/Year Filed)	
			☐
(Number)	(Country)	(Day/Month/Year Filed)	

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

N/A	
(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, C. F. R., Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

PCT/DE98/03794	18 December 1998	Pending
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

Karl Hormann, Esq., Registration No.: 26,470

Send Correspondence to: **Law Offices of Karl Hormann**
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Cambridge, MA 02138-2216

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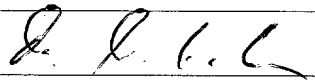
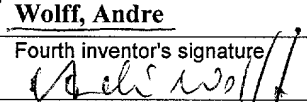
Full name of sole or first inventor **Erzgraeber, Heide B.**	
Sole or first inventor's signature	Date 29 May 2000
Residence **Oderpromenade 4, D-15230 Frankfurt/Oder, Germany** DEX	
Citizenship **German**	
Post Office Address **same as residence**	

Full name of second inventor, if any **Bolze, Klaus-Detlef**	
Second inventor's signature	Date 29 May 2000
Residence **Birkenallee 12, D-15232 Frankfurt/Oder, Germany** DEX	
Citizenship **German**	
Post Office Address **same as residence**	

Full name of third inventor, if any **Grabolla, Thomas**
Third inventor's signature  Date 29 May 2000
Residence **Berendstrasse 25, D-15232 Frankfurt/Oder, Germany** DEX
Citizenship **German**
Post Office Address **same as residence**

Full name of fourth inventor, if any **Wolff, Andre**
Fourth inventor's signature  Date 29 May 2000
Residence **Fischerstrasse 31c, D-15230 Frankfurt/Oder, Germany** DEX
Citizenship **German**
Post Office Address **same as residence**

Full name of fifth inventor, if any
Fifth inventor's signature Date
Residence
Citizenship
Post Office Address

Full name of sixth inventor, if any
Sixth inventor's signature Date
Residence
Citizenship
Post Office Address